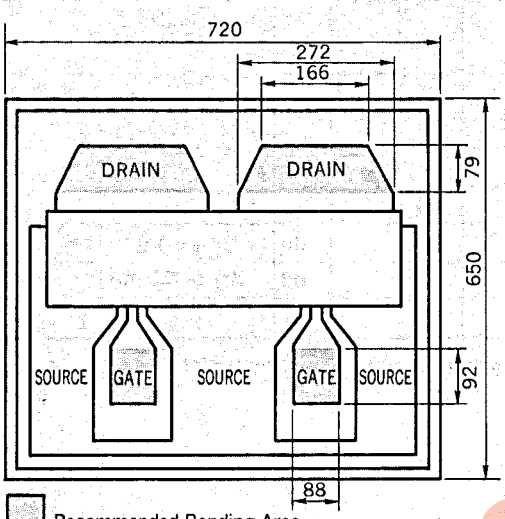
NEC
ELECTRON DEVICE

GaAs MES FET
NE8001

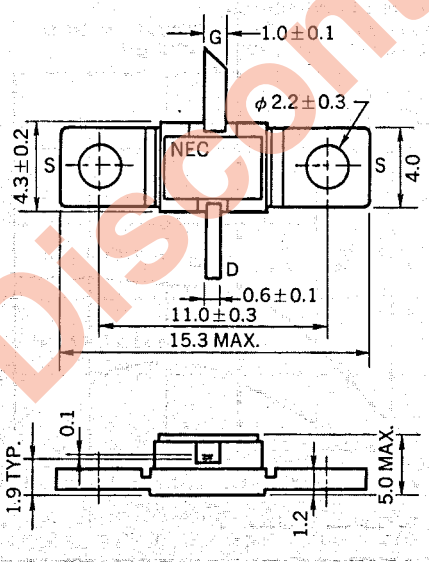
C-BAND MEDIUM POWER GaAs FET
N-CHANNEL GaAs MES FET

PACKAGE DIMENSIONS
NE800100 (CHIP) *1
(Units in mm)



Recommended Bonding Area.
Die Thickness: 110 to 160 μm

PACKAGE CODE-96/99
(Units in mm)



*1 The NE800100 has one good cell on two-cell chip. The waffle pack is marked with a circle to indicate which side of the chip has the good cell.

DESCRIPTION
The NE8001 is a GaAs power FET offering a recessed gate structure which provides high break-down and operating voltages. The device operates with a drain voltage (V_{DS}) of 9 V for CW circuits and up to 13 V for pulsed circuits.

FEATURES
- $P_{O(1\ dB)}$ = 26.0 dBm, G_L = 9.5 dB @ V_{DS} = 9 V
  f = 7.2 GHz (NE800196), 8.4 GHz (NE800199)
- Hermetically sealed package assures high reliability

ORDERING INFORMATION

PART NUMBER	PACKAGE CODE
NE800100	00(CHIP)
NE800196	96
NE800199	99

ABSOLUTE MAXIMUM RATING (T_a = 25 °C)

Drain to Source Voltage	V_{DS}	20	V
Gate to Source Voltage	V_{GS}	−14	V
Drain Current	I_D	0.55	A
Gate Current	I_G	1.5	mA
Total Power Dissipation	P_T	2.5*2	W

*2 T_c = 25 °C

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Saturated Drain Current	I_{DSS}	225	300	400	mA	V_{DS} = 2.5 V, V_{GS} = 0
Pinch-off Voltage	V_P	–2.5	–3.5	–5	V	V_{DS} = 2.5 V, I_D = 2 mA
Transconductance	g_m		60		mS	V_{DS} = 3 V, I_D = 100 mA
Thermal Resistance	R_{th}		60	64	°C/W	channel to case

PERFORMANCE SPECIFICATIONS (T_a = 25 °C)

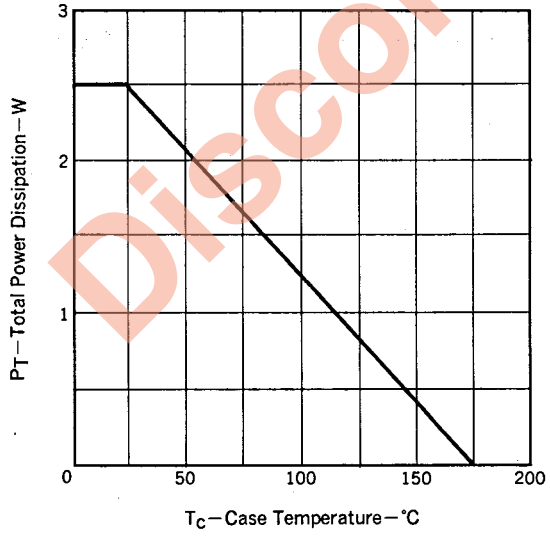
PART NUMBER		NE800100			NE800196			NE800199			UNIT	TEST CONDITIONS	
PACKAGE CODE		CHIP			96			99					
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Output Power*3	P_{out}	25	26		25	26					dBm	V_{DS} = 9 V, $I_D \leqq$ 150 mA	P_{in} = 17.5 dBm, f = 7.2 GHz
								25	26		dBm		P_{in} = 18.0 dBm, f = 8.4 GHz
Output Power at 1 dB Gain Compression Point	$P_{O(1\ dB)}$		26			26					dBm	V_{DS} = 9 V, $I_D \leqq$ 125 mA	f = 7.2 GHz
									26		dBm		f = 8.4 GHz
Linear Gain	G_L		9.5			9.5					dB	V_{DS} = 9 V, $I_D \leqq$ 125 mA	f = 7.2 GHz
									9.5		dB		f = 8.4 GHz
Power Added Efficiency*4	η_{add}		38			38			38		%	$P_{out} = P_{O(1\ dB)}$	

*3 Devices are measured in a tuned amplifier circuit. The drain current I_D is 100 to 150 mA and the gate current is limited below the absolute maximum rating.

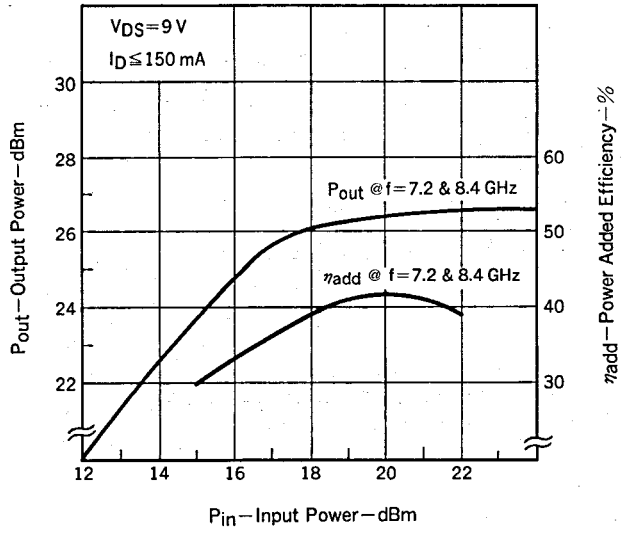
*4 $\eta_{add} = \dfrac{P_{O(1\ dB)} - P_{in}}{V_{DS} \times I_D} \times 100\ (\%)$

TYPICAL CHARACTERISTICS (T_a = 25 °)

POWER DERATING CURVE



NE800196, NE800199
OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER



NE800100 S-PARAMETER (V_{DS} = 9 V, I_D = 150 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.934	–64.1	4.951	137.3	0.046	55.9	0.509	–24.3
2000	0.859	–107.1	3.575	108.0	0.065	34.6	0.413	–41.1
3000	0.828	–134.0	2.674	89.3	0.072	24.0	0.383	–48.3
4000	0.811	–151.2	2.108	73.6	0.073	16.6	0.381	–59.6
5000	0.806	–163.0	1.728	60.9	0.072	14.0	0.389	–70.0
6000	0.801	–172.9	1.454	49.2	0.069	10.2	0.399	–80.1
7000	0.792	179.4	1.250	39.4	0.057	15.5	0.417	–87.8
8000	0.803	171.7	1.109	29.2	0.098	21.3	0.419	–100.3
9000	0.813	166.1	0.996	19.0	0.071	8.3	0.469	–106.4
10000	0.818	160.8	0.893	9.5	0.070	9.7	0.504	–116.5
11000	0.812	155.1	0.814	0.3	0.070	11.0	0.537	–123.6
12000	0.804	148.5	0.727	–9.5	0.070	12.1	0.567	–131.1
13000	0.810	142.2	0.657	–18.1	0.073	13.7	0.597	–138.3
14000	0.820	137.4	0.592	–26.2	0.074	14.3	0.623	–145.9
15000	0.821	134.4	0.532	–33.7	0.074	19.6	0.650	–151.7
16000	0.809	130.1	0.489	–42.0	0.085	20.8	0.677	–156.8
17000	0.781	124.3	0.438	–49.1	0.098	22.2	0.685	–163.8
18000	0.777	118.2	0.405	–56.9	0.111	14.7	0.697	–173.1

NE800196 S-PARAMETER (V_{DS} = 9 V, I_D = 150 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.898	–108.7	4.492	104.8	0.045	32.1	0.402	–45.9
2000	0.851	–152.8	2.816	64.7	0.052	11.1	0.362	–77.8
3000	0.825	–175.6	2.160	35.0	0.053	2.2	0.385	–110.2
4000	0.786	168.3	1.973	7.5	0.051	–1.4	0.458	–135.5
5000	0.678	149.4	2.167	–24.6	0.063	–10.6	0.567	–158.3
6000	0.214	123.0	2.707	–77.9	0.069	–50.9	0.745	174.4
7000	0.654	–142.0	1.846	–154.3	0.019	–154.0	0.692	137.5
8000	0.877	–171.8	0.880	157.8	0.041	66.9	0.588	118.6
9000	0.897	170.9	0.485	120.9	0.069	34.5	0.545	100.6
10000	0.879	156.8	0.310	85.0	0.092	13.9	0.525	83.0

NE800199 S-PARAMETER (V_{DS} = 9 V, I_D = 150 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.903	–88.5	4.972	114.8	0.037	40.4	0.462	–42.3
2000	0.815	–140.0	3.323	71.8	0.045	17.0	0.418	–75.2
3000	0.799	–169.4	2.497	40.3	0.042	9.6	0.425	–107.8
4000	0.788	169.1	2.070	12.4	0.041	13.2	0.485	–135.0
5000	0.766	149.0	1.886	–14.0	0.051	16.7	0.545	–158.3
6000	0.708	124.0	1.878	–42.8	0.065	5.9	0.625	–179.0
7000	0.588	83.6	1.998	–78.4	0.074	–17.3	0.696	158.9
8000	0.457	10.1	2.005	–124.2	0.059	–60.0	0.776	133.1
9000	0.551	–77.3	1.666	–177.3	0.028	173.4	0.760	102.2
10000	0.642	–132.2	1.193	135.9	0.084	85.2	0.680	77.1

CHIP HANDLING

DIE ATTACHEMENT

Die attach can be accomplished with a Au-Sn (300 ± 10 °C) preforms in a forming gas environment. Epoxy die attach is not recommended.

BONDING

Gate and drain bonding wires should be minimum length, semi-hard gold wire (3-8 % elongation) 30 microns or less in diameter. Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Die attach and bonding time should be kept to a minimum. As a general rule, the bonding operation should be kept within a 280 °C — 5 minute curve. If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

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